CLAIMS

1. A flash memory device including a column predecoder, the column predecoder configured to control column selection transistors that select a predetermined bitline from among a plurality of bitlines that are coupled to flash memory cells, the column predecoder comprising:

a buffer unit configured to receive as input an all column selection signal;

decoder units configured to decode an output of the buffer unit and a column address; and

level shifters configured to generate column selection signals that are applied to gates of the column selection transistors in response to an output of the decoder units, wherein the level shifters are configured to apply a high voltage to all the column selection transistors during a stress test in response to the all column selection signal.

2. The flash memory device of claim 2, wherein the buffer unit comprises an inverter.

3. The flash memory device of claim 1, wherein each of the decoder units comprise a NAND gate configured to receive as input the output of the buffer unit and the column address.

4. The flash memory device of claim 1, wherein the level shifters comprise:

first and second PMOS transistors each having a source, a drain, and a gate, wherein the sources of the first and second PMOS transistors are coupled to a high voltage and the gates thereof are cross-coupled to the drains thereof;

an inverter configured to invert the output of the decoder unit;

a first NMOS transistor coupled between the drain of the first PMOS transistor and a ground voltage, with a gate coupled to an output of the inverter; and

a second NMOS transistor coupled between the drain of the second PMOS transistor and the ground voltage, with a gate coupled to the output of the decoder unit, and with a drain coupled to the drain of the second PMOS transistor to generate the column selection signal.

5. The flash memory device of claim 1, further comprising a column decoder that divides the column selection transistors into predetermined stages,

wherein the column decoder comprises:

first-stage column selection transistors configured to select at least two bitlines from among the plurality of bitlines in response to a group of the column selection signals; and

second-stage column selection transistors configured to select a predetermined one of the at least two bitlines in response to another group of the column selection signals and connect the predetermined one of the at least two bitlines with a data line.

6. The flash memory device of claim 5, wherein the column selection transistors are NMOS transistors.

7. The flash memory device of claim 1, wherein the high voltage is provided directly from an external source.

8. The flash memory device of claim 1, wherein the high voltage has a voltage level higher than a power supply voltage.

9. The flash memory device of claim 1, wherein a constant voltage level is applied to the bitline during the stress test.

10. The flash memory device of claim 9, wherein the constant voltage level is a ground voltage level.

11. A stress test method for a flash memory device having column selection transistors configured to select a predetermined bitline from among a plurality of bitlines that are coupled to flash memory cells, the stress test method comprising:

activating a plurality of column selection signals to a high voltage;

applying the plurality of column selection signals to all the column selection transistors;

deactivating all the column selection signals;

turning on selected ones of the column selection transistors in response to deactivating all the column selection signals by decoding a column address.

12. The stress test method of claim 11, wherein activating a plurality of column selection signals to a high voltage comprises providing the high voltage directly from an external source.

13. The stress test method of claim 12, wherein providing the high voltage directly from an external source comprises providing the high voltage with a voltage level higher than a power supply voltage.

14. The stress test method of claim 11, further comprising applying a constant voltage to the plurality of bitlines.

15. The stress test method of claim 14, wherein applying a constant voltage to the plurality of bitlines comprises applying a ground voltage.

16. The stress test method of claim 11, wherein the column selection transistors are NMOS transistors.